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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,374	01/02/2002	Robert C. Glenn	42390P12279	9816
8791	7590	03/28/2005		
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			EXAMINER FILE, ERIN M	
			ART UNIT	PAPER NUMBER
			2634	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/039,374	Applicant(s) ROBERT C. GLENN	
	Examiner Erin M. File	Art Unit 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 January 2002.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-30 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 02 January 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because of inconsistent use of reference characters and naming. An example of this is "150" and "251" have both been used to designate the Highly Linear Phase Interpolator. Further, in figure 1, interrelated *Clock* Signals (146) are output from Highly Linear Phase Interpolator (150) and input to Phase Controller (140). In Figure 2, Interrelated *Control* Signals (254) are output from Phase Controller (220) and input to Highly Linear Phase Interpolator (240).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification and drawing contained within have many instances in which there is disagreement between the description and the accompanying drawings which prohibit the claims from enablement, examples of this include, but are not limited to the following:

- a. On page 6, starting at line 21, the recitation states in description of figure 1, "The phase update logic 130 to generate a control signal(s) 133 for the phase controller 140." However, figure 1 shows control signal(s) (133) generated by phase controller (140) and input to phase logic update (130), contrary to the description in the specification.

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b. On page 6, starting at line 26, the recitation states in description of figure 1, "...phase update logic 130 may generate a control signal 133 comprising a charge signal and a discharge signal to cause the phase controller to increase the voltage of one interrelated control signal 146 while decreasing the voltage of a second interrelated control signal 146." However, figure 1 shows control signals (133) as an input to the phase update logic (130), further, these control signals are output from phase controller (140) which receives interrelated signals (146) as an input, making the control signals (133) unable to increase/decrease the interrelated signals (146)

c. Further in the previous recitation, the interrelated control signals (146), as indicated in the specification as shown as interrelated clock signals in figure 1.

d. On page 7, starting at line 14, the recitation states in description of figure 1, "The phase controller 140 may modify interrelated control signals 146 to cause the highly linear phase interpolator 150 to change the phase of the recovered clock signal 153." Figure 1 does not indicate any way in which interrelated signals (146) are able to effect highly linear phase interpolator (150).

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e. On page 7, starting at line 19, the recitation states in description of figure 1, "...phase controller 140 may output interrelated control signals 146." It is evident from figure 1 that phase controller (146) does not output interrelated control signals (146).

f. On page 7, starting at line 28, the recitation states in description of figure 1, "the phase controller 140 may increase the amplitude of the interrelated control signal 146 associated with the 90 degree reference clock signal and decrease the amplitude of the interrelated control signal 146 associated with the zero degree reference clock signal to cause the highly linear phase interpolator 150 to increase the phase of the recovered clock signal 153 with a substantially linear, or analog, transition." According to the figure, interrelated signal(s) (146) are not input to the highly linear phase interpolator (150) and cannot impact the recovered clock signal (153).

g. On page 8, starting at line 18, the recitation states in description of figure 1, "Other embodiments comprise a phase controller 140 designed to output current signals as interrelated control signals 146." As discussed previously, figure 1 does not indicate phase controller 140 as outputting interrelated control signals (146).

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h. On page 21, starting at line 31, the recitation states in description of figure 5, "The voltage controller 500 may be an embodiment of a phase controller that adjusts a voltage amplitude of an interrelated control signal to adjust the weighting of a reference clock phase." The voltage controller 500 in figure 5 includes outputs interrelated control signals 525, 545, 565, 585, and overflow or trip signals 515, 535, 555, and 575 and no inputs. However these indicated outputs do not agree with the claim of a voltage controller as an embodiment of the phase controller (140) in figure 1. The phase controller (140) in figure 1 indicates interrelated control signals (146) and trip signal(s) (143) as inputs to the phase controller, contrary to the embodiment in figure 5 that indicates these signals are outputs.

i. On page 25, starting at line 4, the recitation states, "Thus, the interrelated control signals 525 and 545 may comprise ramping amplitudes with substantially equivalent slopes. In particular, charge storage circuitry 516 may have an initial charge at a low amplitude boundary and may rise to a high amplitude boundary at substantially the same rate that the charge level on charge storage circuitry 536 decreases from a high amplitude boundary to a low amplitude boundary." The first sentence of this recitation states that the slopes are substantially equivalent, however, the second sentence indicates that the slopes are the negative inverse of each other.

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j. On page 27, starting at line 7, the recitation states, "Referring now to FIG. 6, there is shown an example embodiment of circuitry to substantially maintain a common mode voltage between two control signals, VCA and VCB, output by the voltage controller. Common mode circuitry 600 may comprise inputs VCA and VCB, differential amplifier 610, comparison circuitry 620, having a common mode reference voltage input, common mode logic 630, charge/discharge circuitry A 640 having an output 660 and charge/discharge circuitry B 650 having an output 670." Common mode circuitry (600) of figure 6 is supposed to be the same common mode circuitry (590) of figure 5. The recitation claims control signals VCA and VCB are output by the voltage controller (figure 5, 500), however control signals VCA and VCB are not indicated in any other part of the specification or in the voltage controller as shown in figure 5. Further, the outputs 660 and 670 are not indicated in any way as outputs of the common mode circuitry in Figure 5.


4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin M. File whose telephone number is (571)272-6040. The examiner can normally be reached on M-F 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571)272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erin M. File

3.9.2005

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800